Abstracts

Noise power optimization of monolithic CMOS VCOs

S. Vora and L.E. Larson. "Noise power optimization of monolithic CMOS VCOs." 1999 Radio Frequency Integrated Circuits (RFIC) Symposium 99. (1999 [RFIC]): 167-170.

A small-signal and large-signal analysis was performed on a CMOS microwave VCO and the key contributors to its phase noise were determined. These analyses were verified for a 2.0 GHz, fully integrated L-C VCO in 0.6 /spl mu/m CMOS technology and a phase noise of -103 dBc/Hz at 100 kHz frequency offset with DC power consumption of 22 mW was obtained. These noise analyses can be used to optimize the phase noise of the VCO for a given power consumption.

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